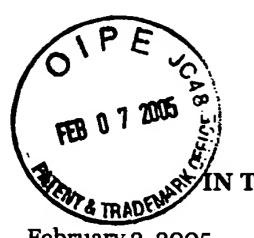
19/419,439.



THE UNITED STATES PATENT AND TRADEMARK OFFICE

February 2, 2005

Patent Number:

6,839,833

January 4, 2005

Title:

÷.

<u>.</u>

₹.

Issued:

System and Method for

Controlling the Entry of Instructions into a Pipeline of

an Instruction Processor

Our File:

RA 5274 (5268)

Customer No.:

Name of Patentees:

27516

Thomas D. Harnett

Leroy J. Longworth

John S. Kuslak

Attn: Certificate of Correction Branch Commissioner for Patents

P O Box 1450

Alexandra, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR PTO MISTAKE (37 C.F.R. § 1.322(a))

- 1. Enclosed, in duplicate, is PTO/SB/44 (also Form PTO-1050), with at least one copy being suitable for printing.
- 2. Enclosed for your ease of reference is a copy of page 2 of the Amendment filed on August 2, 2002, where the error is shown correctly under Please Amend the Application to Read as Follows. The title of the application should read System and Method for Controlling the Entry of Instructions into a Pipeline of an Instruction Processor". Applicant respectfully requests the error be corrected.
- 3. Enclosed for your ease of reference is a copy of page 33 of the Appellant's Brief filed on July 1, 2004, where the error is shown correctly in claim 11. In column 24, line 2 the terms "pipeline-including" should read "pipeline including". Applicant respectfully requests the errors be corrected.
- Please send the Certificate to:

Name:

Unisys Corporation

Beth L. McMahon

Address:

P O Box 64942

MS 4773

St. Paul, MN 55164

Unisys Corporation

(type or print name of assignee)

Signature of person authorized to sign on behalf of assignee

momaker

 \Box

Assignment recorded on October 15, 1999

Reel 010322 Frame 0862

(type or print name of authorized person signing)

Beth L. McMahon

Attorney of Record

Title of authorized person signing

Recorded of assignment attached.

	Recorded of assignment attached.			
		Attached is a "STATEMENT UNDER 37 CFR 3.73(b)," establishing the right of assignee to take action in this case.	f th	

Respectfully submitted,

Best L momalen

Beth L. McMahon Attorney for Applicant Unisys Corporation (MS 4773) P O Box 64942 St. Paul, MN 55164-0942

Reg. No.: 41,987

Tel. No.: (651) 635-7893

BLM/eav

Ì

7

I hereby certify that this correspondence is being deposited in the United States Postal Service as first class mail in an envelope addressed to: Attn: Certificate of Correction Branch, Commissioner for Patents, Alexandria, VA 22313-1450 on February 2, 2005

> <u>Emily Vogt</u> Legal Assistant

February 2, 2005

Date of Signature

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATION OF CORRECTION

PATENT NO : 6,839,833

DATED : January 4, 2005

INVENTOR(S): Thomas D. Hartnett, John S. Kuslak and Leroy J. Longworth

It is certified that error appears in the above-identified patent and that said Letters Patent hereby corrected as shown below:

In the title:

The terms "Pipeline Depth Controller for an Instruction Processor" should read —System and Method for Controlling the Entry of Instructions into a Pipeline of an Instruction Processor—.

In the claims:

Claim number 11, Col. 24, line 2: the terms "pipeline-including" should read --pipeline including

Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATION OF CORRECTION

PATENT NO

6,839,833

DATED

January 4, 2005

INVENTOR(S)

Thomas D. Hartnett, John S. Kuslak and Leroy J. Longworth

It is certified that error appears in the above-identified patent and that said Letters Patent hereby corrected as shown below:

In the title:

The terms "Pipeline Depth Controller for an Instruction Processor" should read —System and Method for Controlling the Entry of Instructions into a Pipeline of an Instruction Processor—.

In the claims:

Claim number 11, Col. 24, line 2: the terms "pipeline-including" should read —pipeline including

PLEASE AMEND THE APPLICATION TO READ AS FOLLOWS:

Please change the title of the Application to "SYSTEM AND METHOD FOR CONTROLLING THE ENTRY OF INSTRUCTIONS INTO A PIPELINE OF AN INSTRUCTION PROCESSOR".

IN THE SPECIFICATION:

5

15

20

10 Please amend the Abstract of the Invention with this paragraph for the paragraph that appears on page 44.

A programmable pipeline depth controller is provided to control the number of instructions that begins execution within an instruction pipeline of an instruction processor within a predetermined period of time. The pipeline depth controller of the present invention includes a logic sequencer responsive to a programmable count value. Upon being enabled, the logic sequencer generates a pipeline control signal to selectively delay the entry of some instructions into the instruction pipeline so that the number of instructions that begins execution within the instruction pipeline during the predetermined period of time following the enabling of the logic sequencer is equal to the count value.

Claim 11:

For use in an instruction pipeline of an instruction processor, the instruction 1 11. processor to execute instructions that are part of the instruction set of the instruction 2 processor, the instruction pipeline being adapted to initiate the execution of a 3 variable number of instructions, up to a predetermined maximum number of 4 instructions, within a predetermined period of time when the instruction pipeline is 5 operating in a default mode, and whereby up to said predetermined maximum 6 number of instructions may be executing simultaneously within the instruction 7 pipeline, the instruction pipeline including a pipeline controller to generate a pipeline 8 control signal for temporarily preventing ones of the instructions from entering the 9 instruction pipeline, a method of utilizing the pipeline controller to control the number 10 of instructions for which execution is initiated by the instruction pipeline within the 11 predetermined period of time, comprising the steps: 12

providing a count to the pipeline controller; and

utilizing the pipeline controller to selectively assert the pipeline control signal to cause the instruction pipeline to initiate the execution of the number of instructions specified by said count within a period of time equal to the predetermined period of time.

<u>Claim 12:</u>

14

15

16

17